

FIG. 1 is a schematic diagram of a circuit and its timing diagram.

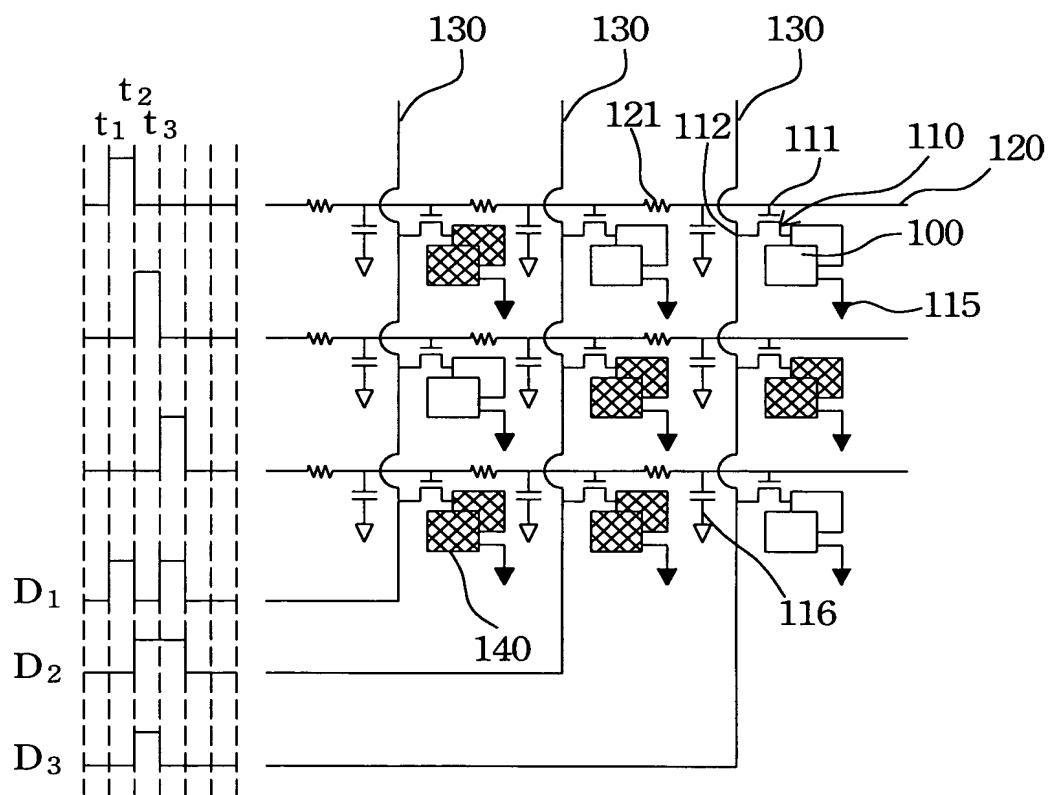


FIG. 1

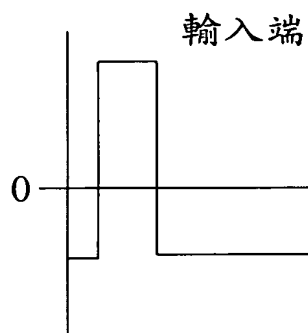


FIG. 2a

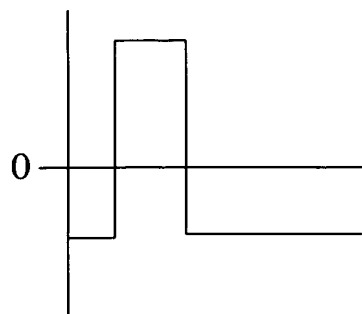


FIG. 2b

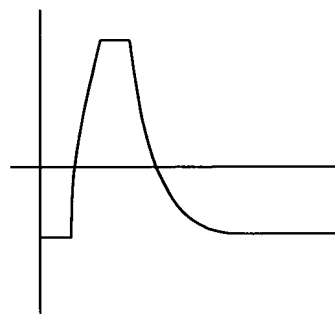


FIG. 2c

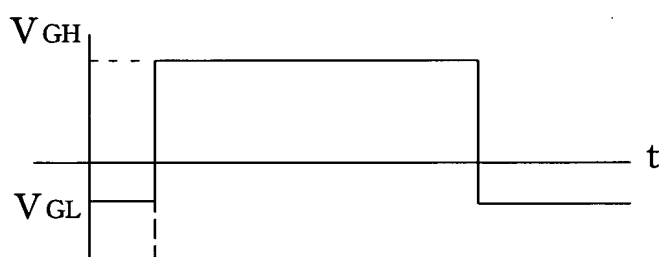


FIG. 3a

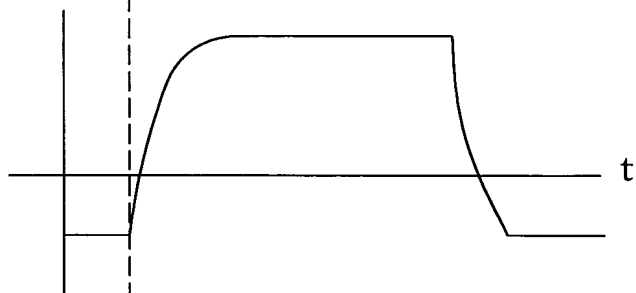


FIG. 3b

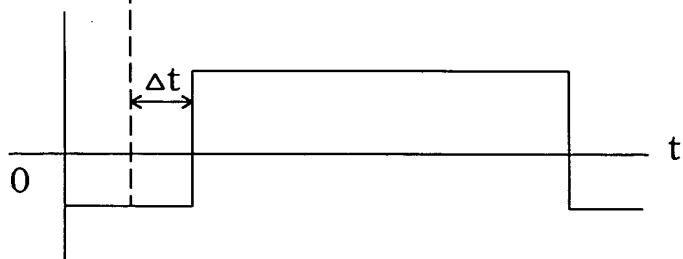
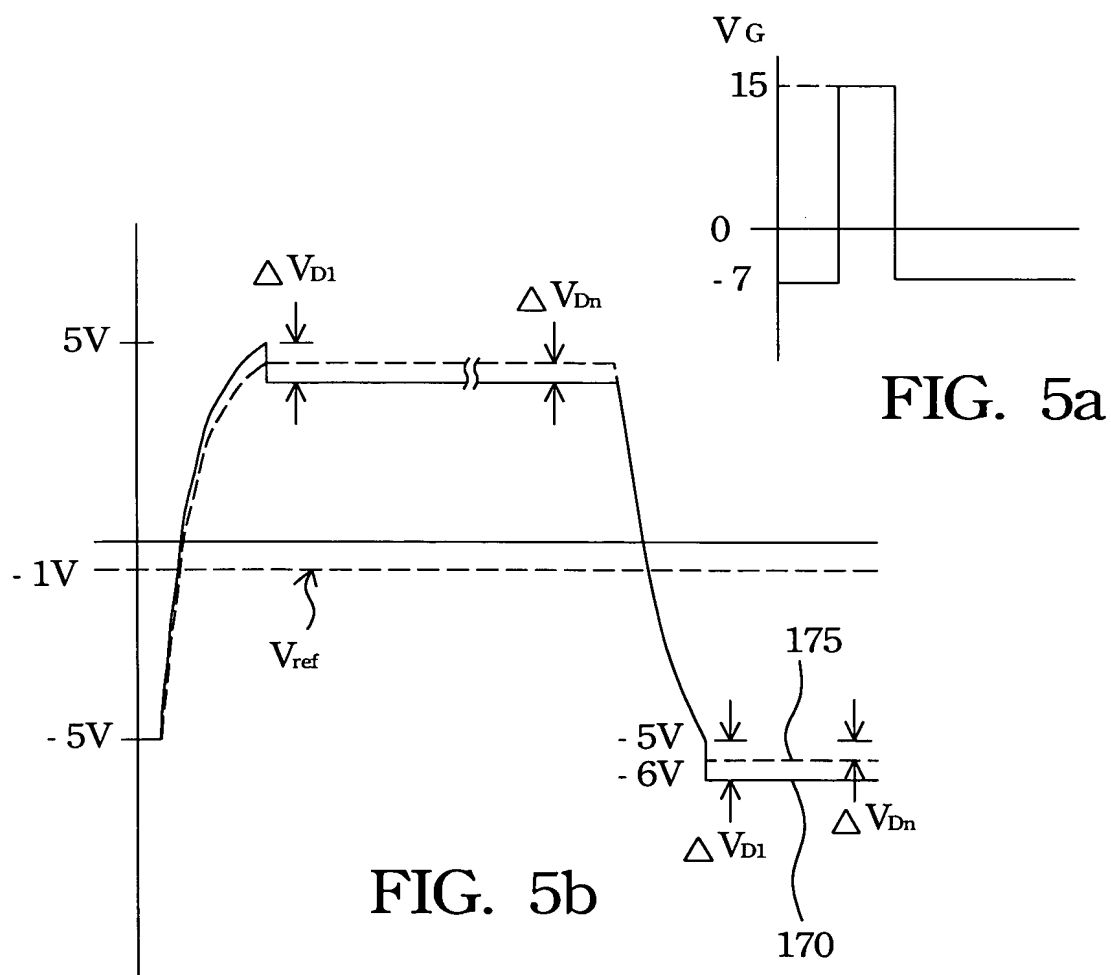
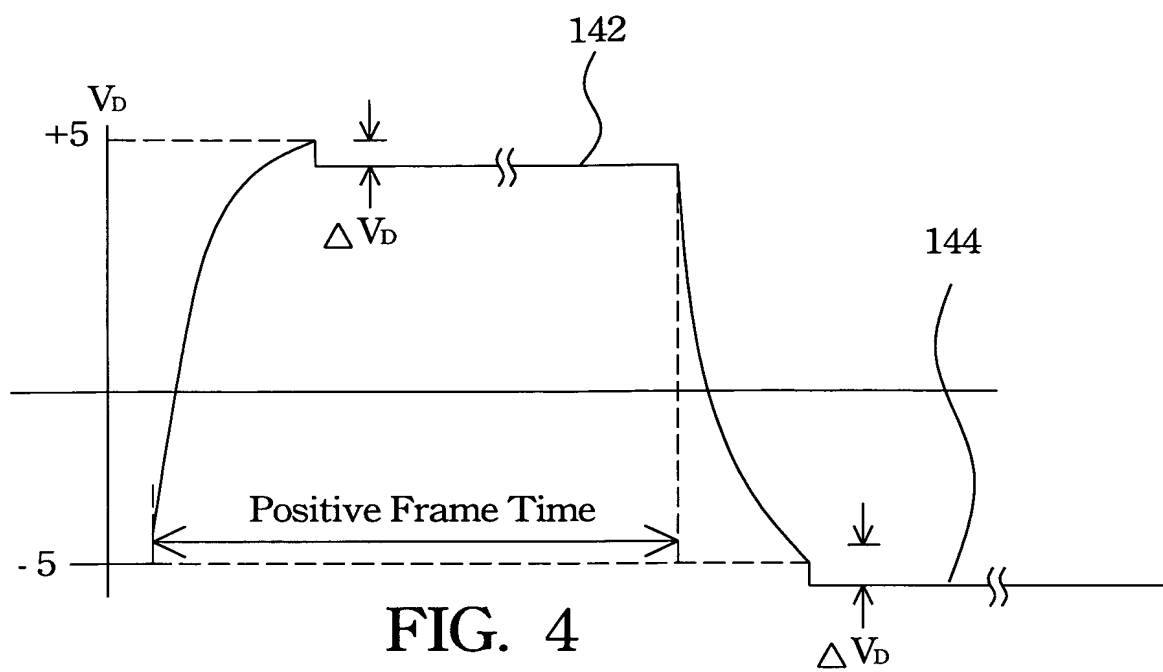


FIG. 3c



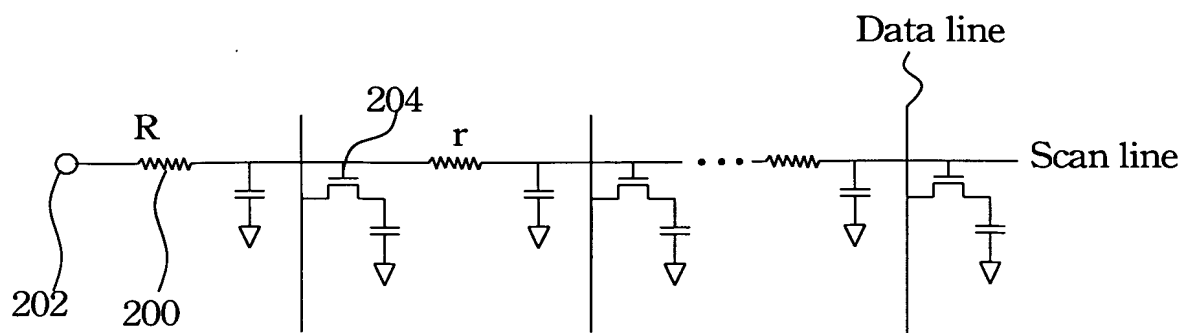


FIG. 6

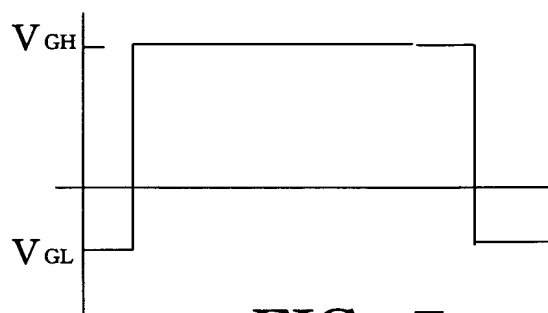


FIG. 7a

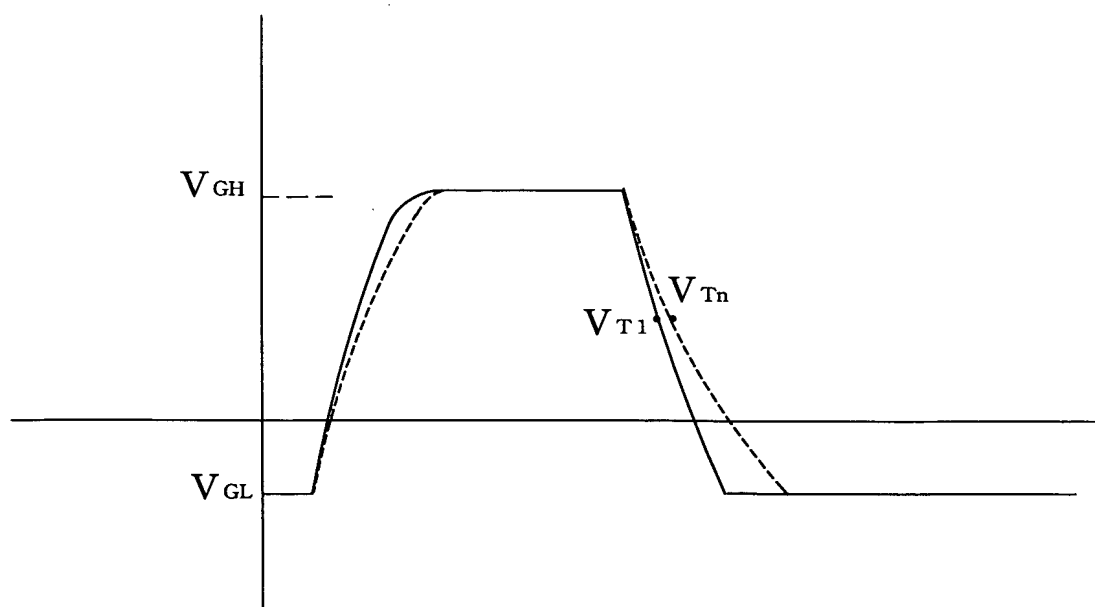


FIG. 7b

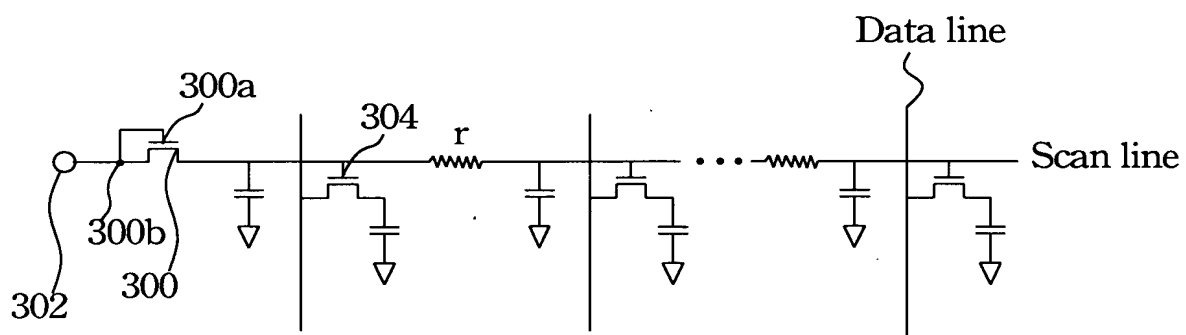


FIG. 8